UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,416	04/23/2001	Kozo Ishida	57454-082	2404

7590 03/25/2004

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
CHARIOUI, MOHAMED	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,416	ISHIDA, KOZO	
	Examiner	Art Unit	
	Mohamed Charioui	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,7 and 8* is/are rejected.

7)☒ Claim(s) *3,4,6,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 1-4** are objected to because of the following informalities: claim 1 recites the limitation "said external input terminals" in page 18, line 6. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim 2 is objected to because of the following informalities: in page 18, lines 20-21, change "a logic level same as the logic level" to --a logic level the same as the logic level--.

Claim 6 is objected to because of the following informalities: in page 20, line 28, change "the taken a plurality" to –the taken plurality--.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishimura et al. (US 4,965,511).

As per claim 1, Nishimura et al. teach an external input terminal for receiving as an input an external test signal in the test mode (see col. 2, lines 10-25); a selecting circuit selecting any of a plurality of internal signals of the semiconductor device in accordance with a test signal input through the external input terminal (see col. 2, lines 10-36 and col. 3, lines 9-27); a plurality of gate circuits provided corresponding to the

plurality of internal signals respectively, each receiving a corresponding internal signal at an input node, and applying the corresponding internal signal to an output node in response to selection of the corresponding internal signal by the selecting circuit (see col. 5, lines 3-15); a signal transmission line connected to the output nodes of the plurality of gate circuits and an external output terminal for externally outputting the internal signal applied to said signal transmission line (see col. 3, lines 47-54).

As per claims 5 and 7, Nishimura et al. further teach an external input terminal receiving as an input an external test signal in said test mode (see col. 2, lines 10-25); a first selecting circuit, selecting one or more of a plurality of first internal signals of the semiconductor device in accordance with the test signal input through the external input terminal (see col. 2, lines 10-36 and col. 3, lines 9-27); a signal generating circuit generating a plurality of first data signals corresponding to the plurality of first internal signals respectively in accordance with the test signal (see col. 3, lines 20-37); a plurality of first gate circuits provided corresponding to the plurality of first internal signals respectively, each receiving at a first input node, the corresponding first internal signal and at a second input node, the corresponding first data signal, applying the corresponding first data signal to an output node when the corresponding first internal signal is selected by the first selecting circuit, and applying the corresponding first internal signal to the output node when the corresponding first internal signal is not selected (see col. 3, lines 9-53); and an internal circuit performing a prescribed operation based on an output signal of the plurality of first gate circuits (see col. 3, line 66 to col. 4, line 23).

As per claim 2 and 8, Nishimura et al. further teach that each gate circuit includes a tristate buffer setting the output node to a logic level same as the logic level of the corresponding internal signal when the corresponding internal signal is selected by the selecting circuit, and sets the output node to a high impedance state when the corresponding internal signal is not selected (see col. 3, lines 47-54).

Allowable Subject Matter

3. **Claims 3, 4, 6, 9 and 10** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and overcoming all the objections.

The following is a statement of reasons for the indication of allowable subject matter: none of the prior art of record teaches or suggests that the selecting circuit includes a designating circuit for designating any of the plurality of groups in accordance with a group designating signal included in the test signal, and a shift register provided corresponding to each group, taking a plurality of data signals included in the test signal in response to designation of the corresponding group by the designating circuit, and applying the taken plurality of data signals to control nodes of a plurality of gate circuits belonging to the corresponding group, in combination with the rest of the claim limitations.

Prior art

4. The prior art made record and not relied upon is considered pertinent to applicant's disclosure:

Yoshimori ['191] discloses testing integrated circuit capable of easily performing parametric test on high pin count semiconductor device.

Kamada ['233] discloses integrated circuit incorporating a test circuit.

Pedersen et al. ['492] disclose integrated circuit clocking technique and circuit therefor.

Sawada ['488] discloses clock synchronous semiconductor memory device capable of preventing outputting of invalid data.

Shibata ['407] discloses integrated circuit probe testing device and method.

Contact information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohamed Charioui whose telephone number is (571) 272-2213. The examiner can normally be reached on 9-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohamed Charioui
3/19/04

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800